CLAIMS

What is claimed is:

1. A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing a layer of Ru on the inter-level dielectric substrate;

depositing a layer of RuO_2 as a diffusion stuffer on the Ru layer; and

depositing copper on the RuO_2 layer.

2. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing multiple layers of Ru and RuO_2 between the inter-level dielectric substrate and the copper layer.

3. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO_2 layer(s) on the Ru layer(s) using an atomic layer deposition technique.

4. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO_2 layer(s) on the Ru layer(s) using a thermal oxidation technique.

5. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO_2 layer(s) on the Ru layer(s) using an electrochemical technique.

6. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 2, further comprising depositing the RuO_2 layer(s) on the Ru layer(s) using physical vapor deposition.

7. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO_2 layer on the Ru layer using an atomic layer deposition technique.

8. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO_2 layer on the Ru layer using a thermal oxidation technique.

9. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO_2 layer on the Ru layer using an electrochemical technique.

10. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 1, further comprising depositing the RuO_2 layer on the Ru layer using physical vapor deposition.

11. A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing a layer of Ir on the inter-level dielectric substrate;

depositing a layer of IrO_2 as a diffusion stuffer on the Ir layer; and

depositing copper on the IrO_2 layer.

12. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing multiple layers of Ir and IrO_2 between the inter-level dielectric substrate and the copper layer.

13. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO_2 layer(s) on the Ir layer(s) using an atomic layer deposition technique.

14. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO_2 layer(s) on the Ir layer(s) using a thermal oxidation technique.

15. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO_2 layer(s) on the Ir layer(s) using an electrochemical technique.

16. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 12, further comprising depositing the IrO_2 layer(s) on the Ir layer(s) using physical vapor deposition.

17. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO_2 layer on the Ir layer using an atomic layer deposition technique.

18. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO_2 layer on the Ir layer using a thermal oxidation technique.

19. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO_2 layer on the Ir layer using an electrochemical technique.

20. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 11, further comprising depositing the IrO_2 layer on the Ir layer using physical vapor deposition.

21. A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing a layer of Ir on the inter-level dielectric substrate;

depositing a layer of RuO_2 as a diffusion stuffer on the Ir layer; and

depositing copper on the RuO_2 layer.

22. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 21, further comprising depositing multiple layers of Ir and RuO_2 between the inter-level dielectric substrate and the copper layer.

23. A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing a layer of Ru on the inter-level dielectric substrate;

depositing a layer of IrO_2 as a diffusion stuffer on the Ru layer; and

depositing copper on the IrO_2 layer.

24. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 21, further comprising depositing multiple layers of Ru and IrO_2 between the inter-level dielectric substrate and the copper layer.

25. A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing one or a plurality of layers of RuO_2 on the inter-level dielectric substrate; and

depositing copper on the RuO_2 layer.

26. The method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits of Claim 25, further comprising depositing the RuO_2 layer on the inter-level dielectric using an atomic layer technique.

27. The method of controlling and containing copper diffusion during the integration of copper interconnects during fabrication of integrated circuits of Claim 25, further comprising depositing the RuO_2 layer on the inter-level dielectric using an electrochemical technique.

28. The method of controlling and containing copper diffusion during the integration of copper interconnects during fabrication of integrated circuits of Claim 25, further comprising depositing the RuO_2 layer on the inter-level dielectric using a thermal oxidation technique.

29. The method of controlling and containing copper diffusion during the integration of copper interconnects during fabrication of integrated circuits of Claim 25, further comprising depositing the RuO_2 layer on the inter-level dielectric using a physical vapor technique.

30. A method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing one or a plurality of layers of Ir/Ru on the inter-level dielectric substrate; and

depositing one or a plurality of layers of IrO_2/RuO_2 on the Ir/Ru layers; and

depositing copper on the IrO_2/RuO_2 layers.

31. A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ru as a diffusion barrier.

32. The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 31, further comprising eliminating a copper seed layer.

33. A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ru and RuO_2 as a diffusion barrier.

34. The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 33, further comprising eliminating a copper seed layer.

35. A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ir as a diffusion barrier.

36. The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 35, further comprising eliminating a copper seed layer.

37. A method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ir and IrO_2 as a diffusion barrier.

38. The method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication of Claim 37, further comprising eliminating a copper seed layer.

39. An integrated circuit, comprising:

a plurality of semiconductor devices;

the plurality of semiconductor devices being coupled via copper interconnects;

the copper interconnects being deposited on one or a plurality of Ru layer(s);

the Ru layer(s) being deposited on one or a plurality of RuO_2 layer(s); and

the RuO_2 layer(s) being deposited on an inter-level dielectric.

40. The integrated circuit of Claim 39, further comprising the semiconductor devices and copper interconnects having sub-micron features.

41. An integrated circuit, comprising:

a plurality of semiconductor devices;

the plurality of semiconductor devices being coupled via copper interconnects;

the copper interconnects being deposited on one or a plurality of Ir layer(s);

the Ir layer(s) being deposited on one or a plurality of IrO_2 layer(s); and

the IrO_2 layer(s) being deposited on an inter-level dielectric.

42. The integrated circuit of Claim 41, further comprising the semiconductor devices and copper interconnects having sub-micron features.

43. An integrated circuit, comprising:

a plurality of semiconductor devices;

the plurality of semiconductor devices being coupled via copper interconnects;

the copper interconnects being deposited on one or a plurality of Ru layer(s);

the Ru layer(s) being deposited on one or a plurality of IrO_2 layer(s); and

the IrO_2 layer(s) being deposited on an inter-level dielectric.

44. The integrated circuit of Claim 43, further comprising the semiconductor devices and copper interconnects having sub-micron features.

45. An integrated circuit, comprising:

a plurality of semiconductor devices;

the plurality of semiconductor devices being coupled via copper interconnects;

the copper interconnects being deposited on one or a plurality of Ir layer(s);

the Ir layer(s) being deposited on one or a plurality of RuO_2 layer(s); and

the RuO_2 layer(s) being deposited on an inter-level dielectric.

46. The integrated circuit of Claim 45, further comprising the semiconductor devices and copper interconnects having sub-micron features.